

VARIABLE DATA WIDTH OPERATION IN MULTI-GIGABIT TRANSCEIVERS
ON A PROGRAMMABLE LOGIC DEVICE

ABSTRACT

A transmit variable-width interface can be programmed to convert an electronic digital data path that is either $1N$, $2N$, $4N$, or $8N$ bits wide into a data path that is $2N$ bits wide, either by serializing bits ($4N$ - or $8N$ -bit cases), re-clocking bits ($2N$ -bit case), or grouping bits ($1N$ -bit case). A receive variable-width interface can be programmed to convert a data path $2N$ bits wide into a data path that is $1N$, $2N$, $4N$, or $8N$ bits wide. The widths of the two variable-width data paths are controlled independently. The variable-width interfaces are coupled between a multi-gigabit transceiver and core logic of a programmable logic device. The incoming and outgoing data paths of the variable-width interfaces have separate clocks signals that are synchronized such that small amounts of skew in these clock signals do not disrupt the operation of the variable-width interfaces.